that in Fig. 2.-- before "Fig. 4 is a schematic", and change "Fig. 4 is a schematic" to --Fig. 5 is a schematic--; and

line 12, change "Fig. 5" to --Fig. 6--.

IN THE CLAIMS:

Amend Claim 9 as follows:

~~9.~~ (Once amended) A Miller-compensated amplifier, for amplifying an input signal applied to an amplifier input node to provide an output signal at an amplifier output node, comprising:

a first amplifier stage having an internal node as an input thereto, and having a first stage output node;

a second amplifier stage having said amplifier input node as an input thereto, and having a second stage output node;

a third amplifier stage having a third stage input node coupled to said first stage output node and to said second stage output node, and providing said output signal at said amplifier output node; and

a capacitor coupled between said amplifier output node and said internal node so as to provide voltage-mode gain.

Add the following new Claims 10 - 13:

~~10.~~ A Miller-compensated amplifier according to Claim ~~9~~ 1, wherein said capacitor is connected such that a left-hand-plane zero is provided in said compensated amplifier.

3 ~~11.~~ A compensated amplifier according to Claim 2 ~~10~~, wherein said left-hand-plane zero is selected so as to optimize compensation for said compensated amplifier.

4 ~~12.~~ A compensated amplifier according to Claim 1 ~~9~~, wherein said first amplifier stage comprises a diode connected transistor and a ratioed transistor connected together forming a current mirror, and wherein said diode connected transistor senses said capacitive current at said internal node and said ratioed transistor amplifies said capacitive current.

5 ~~13.~~ A Miller-compensated amplifier, for amplifying a differential input signal applied to an amplifier input node to provide an output signal at an amplifier output node, comprising:

a differential amplifier, for converting the voltage of said differential input signal to differential input currents;

a bias voltage source;

a first FET and a second FET;

first and second current mirrors each mirroring one of said differential input currents to one of said first and said second FETs, said first current mirror comprising a third FET and a fourth FET having a common gate connection node, and said second current mirror comprising a fifth FET and a sixth FET having a common gate connection node;

a third current mirror providing current to said first FET and to said second FET;

a seventh FET sensing, at a gate thereof, a voltage on one of said first FET and said second FET, and having a source thereof connected to a voltage source;